100-V, 3-A/6-A, Half Bridge GaN Driver with Integrated Bootstrap Diode

Features

- Floating Supply for Bootstrap Operation to + 100 V
- Integrated Bootstrap Diode for Floating Supply
- Supply Voltage Range from 4.5 V to 5 V for GaN FET
- 3-A Peak Source, 6-A Sink Output Current Capability
- Split Outputs for Adjustable Turn-on, Turn-off Strength
- Fast Propagation Delay with
  - Typical 24 ns
  - Maximum 2.9 ns Delay Matching
- Two Control Input Mode
  - Single PWM Input with programmable dead-time
  - Independent Input with shoot-through prevention
- Minimum CMTI of 50 V/ns dv/dt
- Protections
  - Under voltage protection
  - Shoot-Through Prevention

Applications

- Switch-Mode Power Supplies
- Motor Control and Drives
- Solar Power Inverters
- Etc

Description

This document contains detailed specifications of the SMA6533 is a half-bridge GaN gate driver with 3-A/6-A source and sink peak current respectively. They are designed for fast switching to drive enhancement-mode Gallium Nitride (GaN) FETs in a synchronous buck, boost, or half-bridge configuration. The device has an integrated 100 V bootstrap diode and inputs for the high-side and low-side outputs for maximum control flexibility. The high-side bias voltage is generated using a bootstrap technique and is internally clamped, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement-mode GaN FETs. The SMA6533 has split-gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently. SMA6533 offers short and matched propagation delays. The SMA6533 features two control input modes such as independent input mode with shoot-through prevention and single PWM input mode with dead-time between the high and low-side driver.

Device Information

Part Number	Package	Body Size
SMA6533-W	WLCSP	1.71 mm x 1.71 mm

Simplified Block Diagram

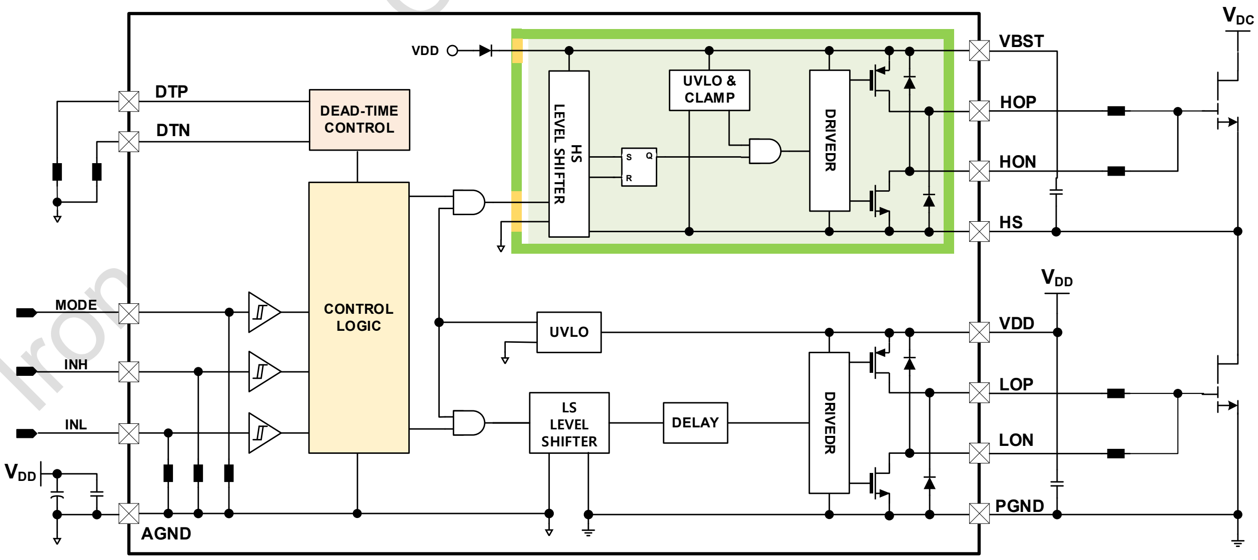


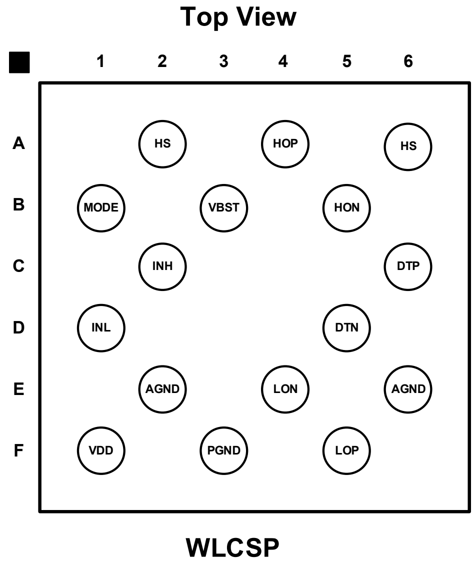
Figure 1. Simplified Block Diagram

Notes

1) The bypass capacitor recommended using 2 capacitors at least 100 nF ceramic surface-mount type and few microfarads added in parallel between V_{DD} and AGND and the other bypass capacitors between V_{DD} and PGND

Contents

Pin Assignments



16 Pin, 1.71 mm x 1.71 mm - WLCSP

Figure 2. Pin Assignments

Pin Description

Pin Number	NAME	I/O	Description
E2[2)]	AGND	G	**Ground for analog** (all input signals are referenced to this ground)
D1	INL	I	**Low side signal input**
C2	INH	I	**High side signal input**
B1	MODE	I	**Input mode control**
A2[2)]	HS	G	**Ground for high side gate driver**
B3	VBST	P	**Bootstrap for high side Output**
A4	HOP	O	**High side current source output**
B5	HON	O	**High side current sink output**
A6[2)]	HS	G	**Ground for high side gate driver**
C6	DTP	A	**Dead time resister for high side rising edge**
D5	DTN	A	**Dead time resister for low side rising edge**
E6[2)]	AGND	G	**Ground for analog**
F5	LOP	O	**Low side current source output**
E4	LON	O	**Low side current sink output**
F3	PGND	G	**Ground for power stage**
F1	VDD	P	**Power supply**

*P: Power, G: Ground, O: Output, I: Input, A: Analog

Notes

2) E2 and E6, A2 and A6 pins are internally connected

Functional Diagram

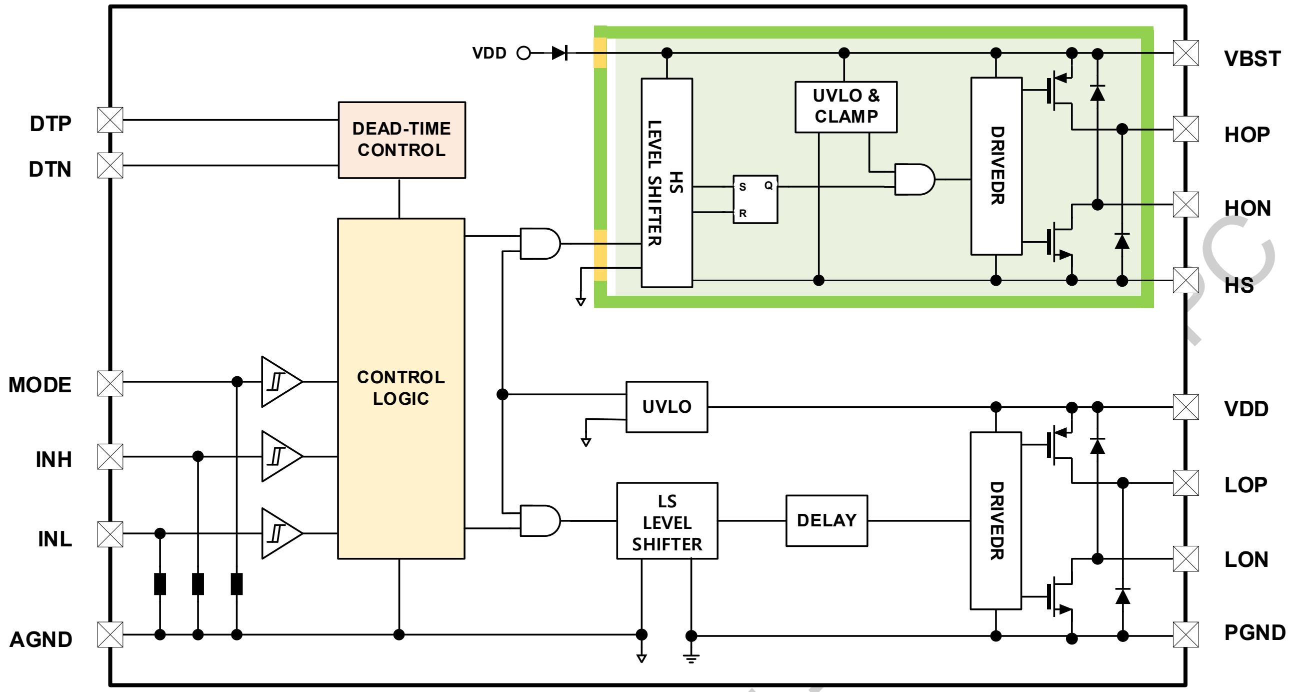


Figure 3. Functional Diagram

Absolute Maximum Ratings

Stress(es) beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only. It does not imply the functional operation of the device or other conditions beyond those is indicated in the following. Exposure to absolute maximum rating condition(s) for extended periods may affect device reliability.

Parameter	Lower Limit	Upper Limit	Unit
Low side Supply Voltage (VDD) to AGND[3)]	-0.3	7	V
Floating Supply Voltage (VBST) to HS[4)]	-0.3	6	V
Floating Supply Offset Voltage (HS) to AGND[3)]	-5	100	V
High side Output Voltage (HOP and HON) to HS[4)]	V_{HS}-0.3	V_{BST} + 0.3	V
Low side Output Voltage (LOP and LON) to PGND[5)]	-0.3	V_{DD} + 0.3	V
Input Voltage (INH, INL, MODE) to AGND[3)]	-0.3	V_{DD} + 0.3	V
Human Body Model (HBM) ESD[6)]	-2000	2000	V
Charged Device Model (CDM) ESD	-1000	1000	V
Operating Ambient Temperature	-40	125	°C
Operating Junction Temperature	-40	125	°C
Storage Ambient Temperature	-65	150	°C
Lead Soldering Temperature (within 10 sec)		300	°C

Notes

3) All voltage values are given with respect to AGND pin
4) All voltage values are given with respect to HS pin
5) All voltage values are given with respect to PGND pin
6) This device series incorporates ESD protection and is tested by the following methods
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001-2017 for all pins
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-002-2018 for all pins
   Latch up Current Maximum Rating: ≤100 mA per JEDEC standard JESD78F:2022

Thermal Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient[7) & 8)]	$R_{\Theta JA}$		55		°C/W
Thermal Resistance Junction-to-case (top) thermal resistance	Ψ_{JT}		0.05		°C/W
Thermal Resistance Junction-to board thermal resistance	Ψ_{JB}		15.6		°C/W

Notes

7) T_A = 25 °C for WLCSP package
8) Board condition complied with JESD51-9 standard
   Mounted on 101.5 mm x 114.5 mm x 1.6 mm FR4 substrate with a 4-layer (2s2p)
   Copper thickness: 50 um (1.43 oz) for Top & Bottom layer and 35 um (1 oz) for inner plane
   Natural convection (still air) condition

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage[9)]	V_{DD}	4.5	5.0	5.5	V
Input Voltage (INH, INL, MODE)	VIN	-0.3	5.0	5.5	V
Floating Supply Offset Voltage	HS	-5		90	V
Floating Supply Voltage[9)]	V_{BST}	V_{HS} + 4		V_{HS} + 5.5	V
Common-mode Transient Immunity	CMTI	50			V/ns

Notes

9) V_{DD} and V_{BST} UVLO threshold voltage with respect to AGND and HS pins respectively.

Electrical Characteristics - DC

V_{DD} = V_{BST} = 5 V, HS = 0 V, No load on LOP and LON or HOP and HOL. Typical values and limits appearing in normal type apply for T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
V_{DD} quiescent current	I_{DDQ1}	MODE= INH=INL=Low	15	30	40	µA
	I_{DDQ2}	MODE = INH=INL= High	150	250	350	µA
V_{DD} operating current	I_{DDO}	f_{IN} = 500 kHz		0.67		mA
V_{BST} quiescent current	I_{VBSTQ1}	MODE= INH=INL=Low	10	25	40	µA
	I_{VBSTQ2}	MODE = INH=INL = High	30	45	65	µA
V_{BST} to PGND leakage current	I_{LKBST}	VBST=HS=100 V			100	nA
V_{BST} operating current	I_{VBSTO}	f_{IN} = 500 kHz		0.6		mA
VDD UVLO Protection						
UVLO Threshold+	V_{DDUV+}	V_{DD} rising	3.4	3.85	4.3	V
UVLOL Threshold –	V_{DDUV-}	V_{DD} falling	3.1	3.6	4	V
Hysteresis	V_{DDHYS}			0.25		V
VBST UVLO Protection						
UVLO Threshold+	V_{BSTUV+}	V_{BST} rising	2.9	3.3	3.8	V
UVLO Threshold-	V_{BSTUV-}	V_{BST} falling	2.6	3.05	3.5	V
Hysteresis	$V_{VBSTHYS}$			0.25		V
Dead-Time Control in PWM Input Mode						
Dead-time for Low Side Output	t_{DTN20}	R_{DTN} = 20 kΩ	1.8	2.8	3.8	ns
	t_{DTN100}	R_{DTN} = 100 kΩ	13.3	16.3	19.3	ns
Dead-time for High Side Output	t_{DTP20}	R_{DTP} = 20 kΩ	0.4	1.4	2.4	ns
	t_{DTP100}	R_{DTP} = 100 kΩ	11.5	14.5	17.5	ns
Dead-time Mismatching	M_{DT20}	R_{DTN} = R_{DTP} = 20 kΩ	0.5	1.5	2.5	ns
	M_{DT100}	R_{DTN} = R_{DTP} = 100 kΩ	0.4	1.7	3	ns
Input Logic (INH, INL and MODE)						
Input High Threshold Voltage	V_{INH}			1.9	2.4	V
Input Low Threshold Voltage	V_{INL}		1.1	1.4		V
Input Hysteresis Voltage	V_{INHYS}			0.5		V
High Input Leakage Current	I_{LKH}	V_{INH} = V_{INL} = 5 V	22	27	32	µA
Low Input Leakage Current	I_{LKL}	V_{INH} = V_{INL} = 0 V	-1		1	µA
Input Pulldown Resistance	R_{INPD}		157	185	228	kΩ
Bootstrap Diode						
Bootstrap Diode Voltage	V_{DL}	I = 100 µA		0.64		V
	V_{DH}	I = 100 mA		0.98		V
VBST-HS Clamp Voltage	$V_{BST, CLAMP}$	I = 1 mA		5.75		V

Electrical Characteristics – DC and AC

V_{DD} = V_{BST} = 5 V, HS = 0 V, No load on LOP and LON or HOP and HOL. Typical values and limits appearing in normal type apply for T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Short Circuit Clamp						
Clamping Voltage (V_{LON}-V_{DD} or V_{HON}-V_{BST})	$V_{CLAMP\text{-}OUTH}$	LON=HON=Open, t_{CLP} = 10 us, I_{HOP}=I_{LOP} or I_{CLAMP} = 500 mA	1.2	1.7	2.5	V
Clamping Voltage (PGND=V_{LOP} or HS-V_{HOP})	$V_{CLAMP\text{-}OUTL}$	LOP=HOP=Open, t_{CLP} = 10 us, I_{HON}=I_{LON} or I_{CLAMP}= 500 mA	1.2	1.7	2.5	V
Gate Driver						
High Output Transistor $R_{DS\ (ON)}$	ROH	I_{OUT} = 100 mA		0.65		Ω
Low Output Transistor $R_{DS\ (ON)}$	ROL	I_{OUT} = 100 mA		0.23		Ω
Peak Source Current [10)]	IO+	HOP, LOP = 0 V		3		A
Peak Sink Current [10)]	IO-	HON, LON = 5 V		6		A
Switching Parameters						
Propagation Delay	t_{PLH}, t_{PHL}		23	24	26	ns
Propagation Delay Mismatch	MT	$\| t_{PLH} – t_{PHL} \|$		1.8	2.9	ns
Rise time	t_R	C_{LOAD} = 1000 pF		5.5		ns
Fall time	t_F	C_{LOAD} = 1000 pF		4.5		ns
Minimum Input Pulse Width that Changes The Output	$t_{PW,MIN}$		15			ns

Notes

10) Guaranteed by design

Typical Characteristics

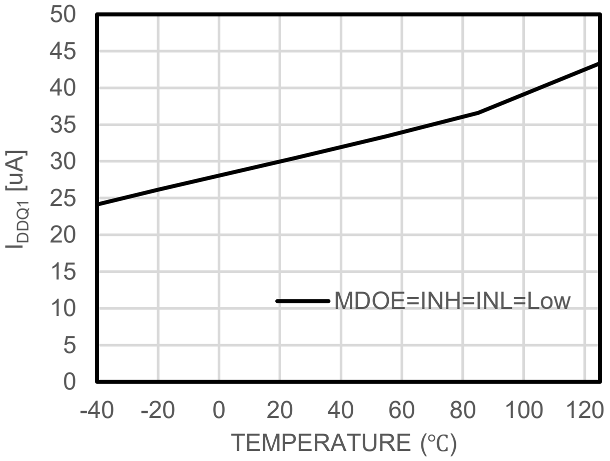


Figure 4. V_{DD} quiescent current vs. Temperature

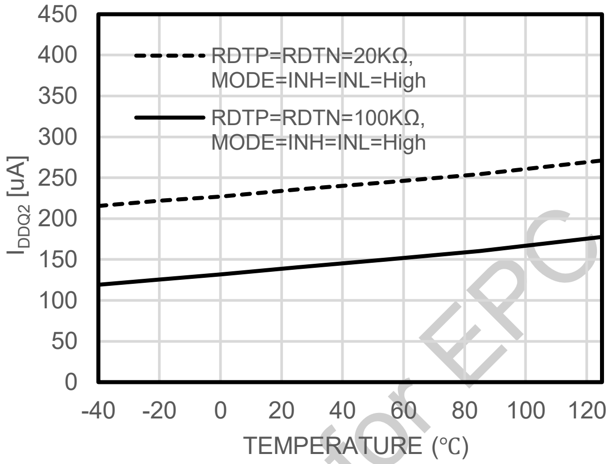


Figure 5. V_{DD} quiescent current vs. Temperature

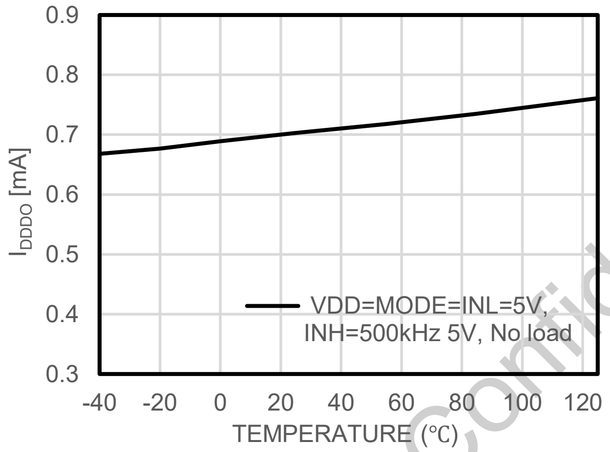


Figure 6. V_{DD} Operating current vs. Temperature

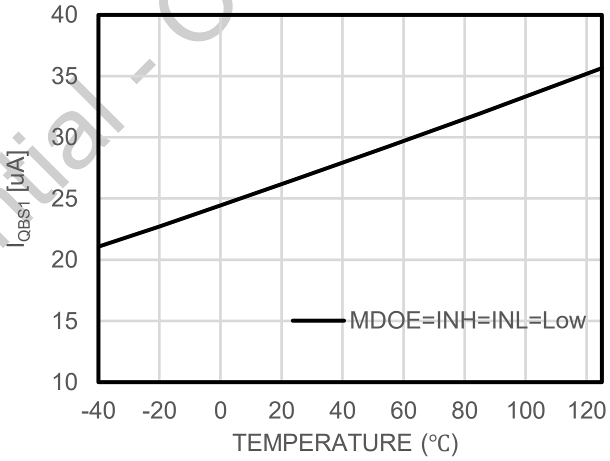


Figure 7. V_{BST} quiescent current vs. Temperature

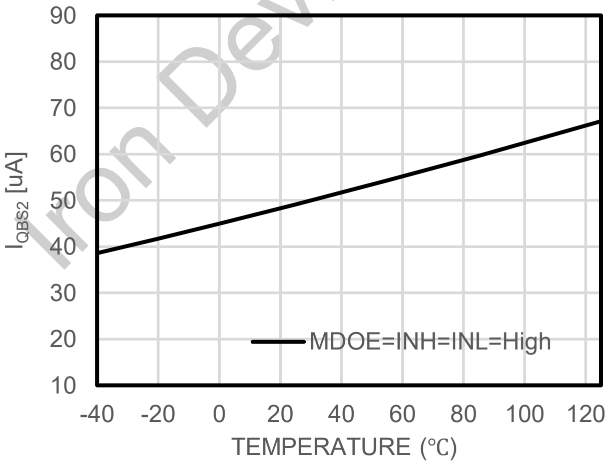


Figure 8. V_{BST} quiescent current vs. Temperature

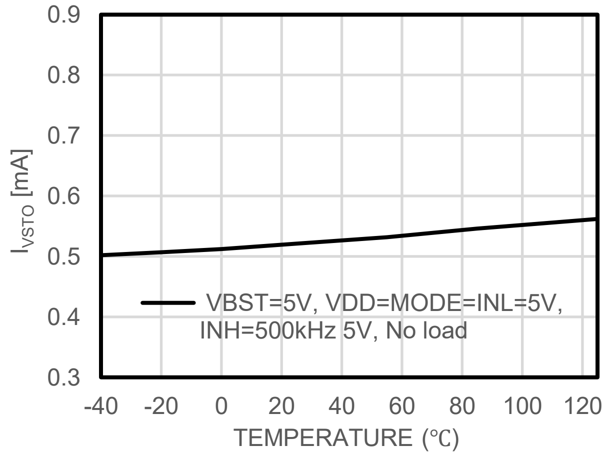


Figure 9. V_{BST} operating current vs. Temperature

Typical Characteristics (Continued)

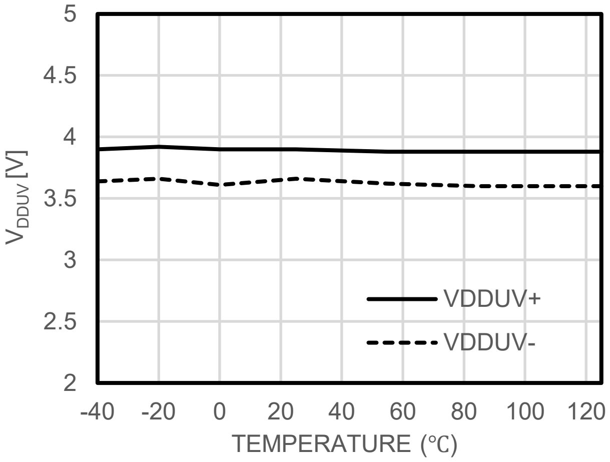


Figure 10. V_{DD} UVLO Threshold vs. Temperature

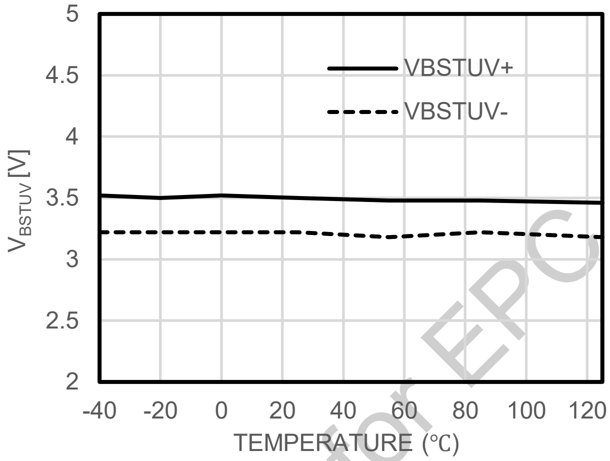


Figure 11. V_{BST} UVLO Threshold vs. Temperature

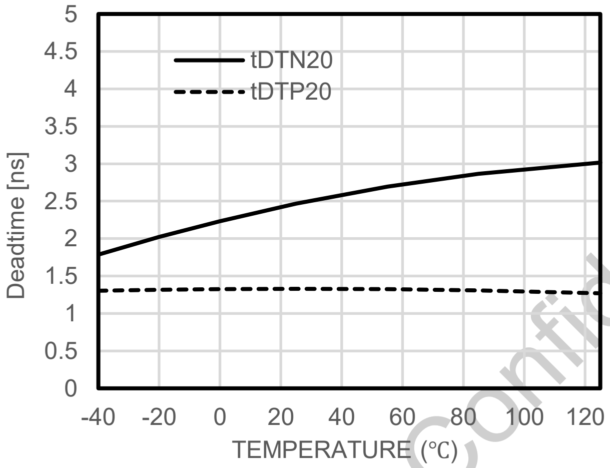


Figure 12. Deadtime (R_{DTP}=R_{DTN} =20kΩ) vs. Temperature

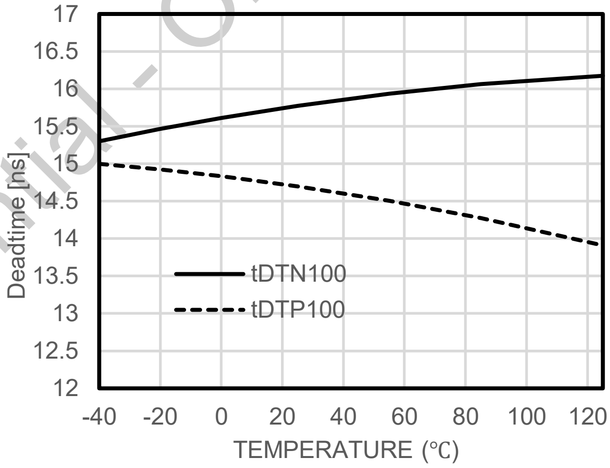


Figure 13. Deadtime (R_{DTP}=R_{DTN} =100kΩ) vs. Temperature

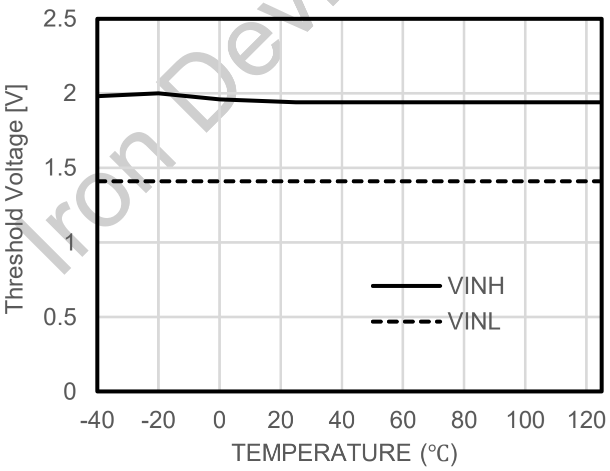


Figure 14. Input High Threshold Voltage vs. Temperature

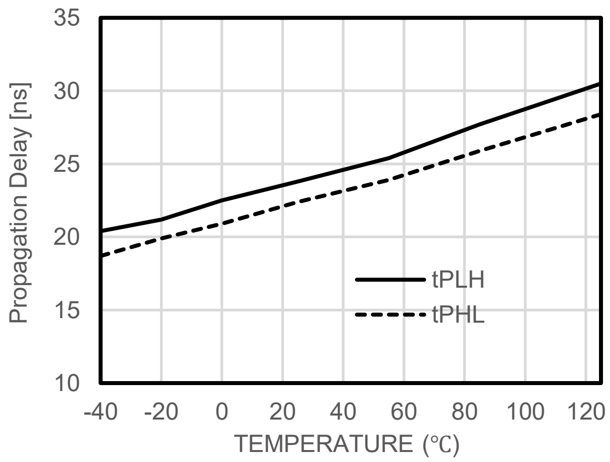


Figure 15. INL Propagation Delay vs. Temperature

Typical Characteristics *(Continued)*

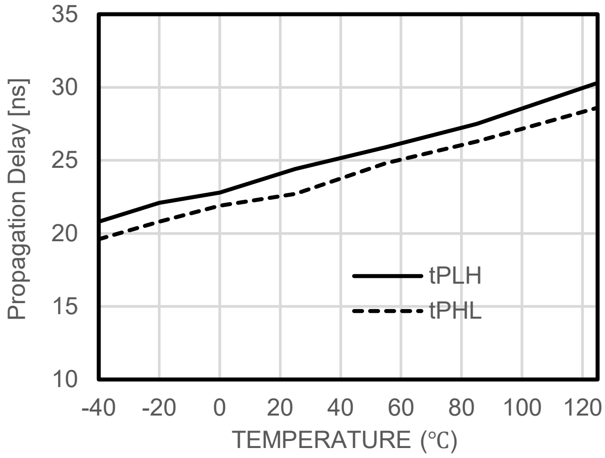


Figure 16. INH Propagation Delay vs. Temperature

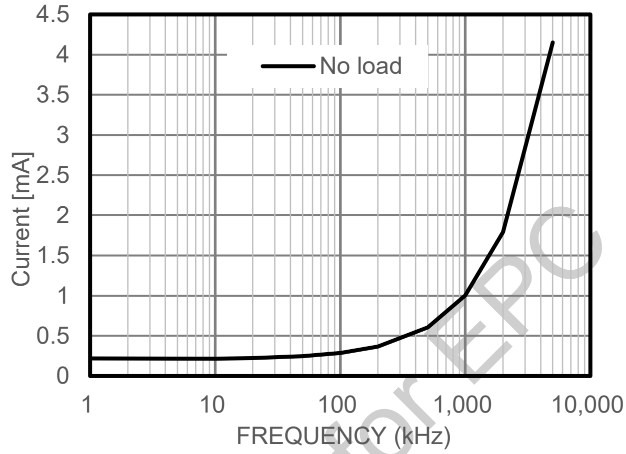


Figure 17. V_{DD} operating current (No load) vs. Frequency

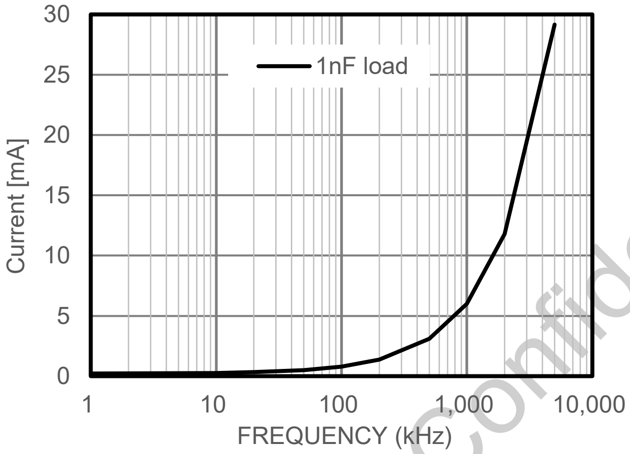


Figure 18. V_{DD} operating current (1nF load) vs. Frequency

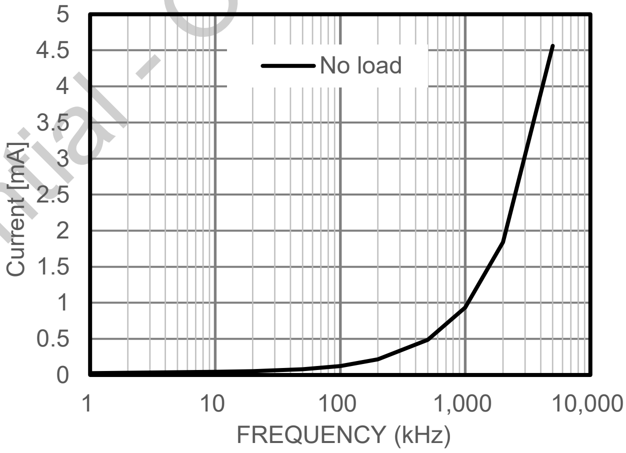


Figure 19. V_{BST} operating current (No load) vs. Frequency

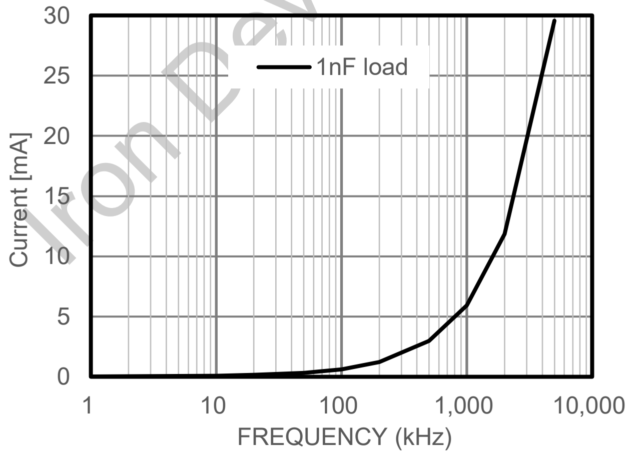


Figure 20. V_{BST} operating current (1nF load) vs. Frequency

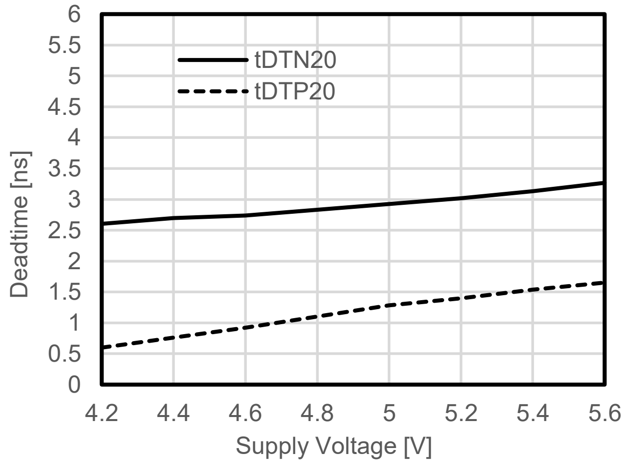


Figure 21. Deadtime (R_{DTP}=R_{DTN} =20kΩ) vs. Supply Voltage (V_{DD}=V_{BST})

Typical Characteristics *(Continued)*

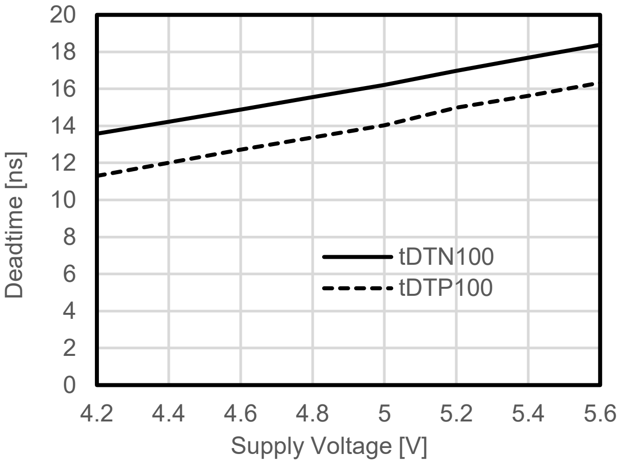


Figure 22. Deadtime (R_{DTP}=R_{DTN} =100kΩ) vs. Supply Voltage (V_{DD}=V_{BST})

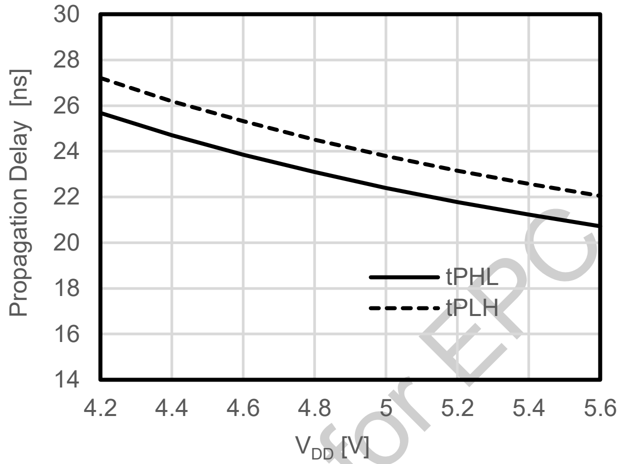


Figure 23. INL Propagation Delay vs. Supply Voltage (V_{DD}=V_{BST})

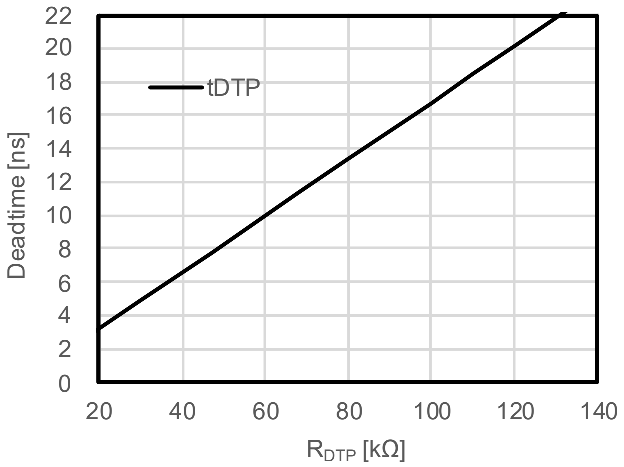


Figure 24. t_{DTP} Deadtime vs. R_{DTP} (V_{DD}=5V, V_{BST}=4.3V)

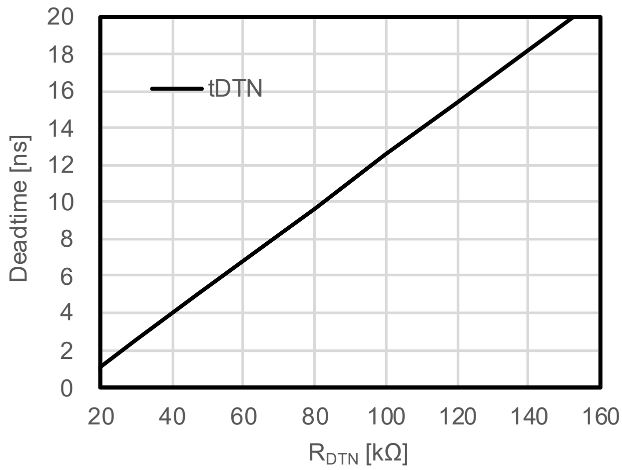


Figure 25. t_{DTN} Deadtime vs. R_{DTN} (V_{DD}=5V, V_{BST}=4.3V)

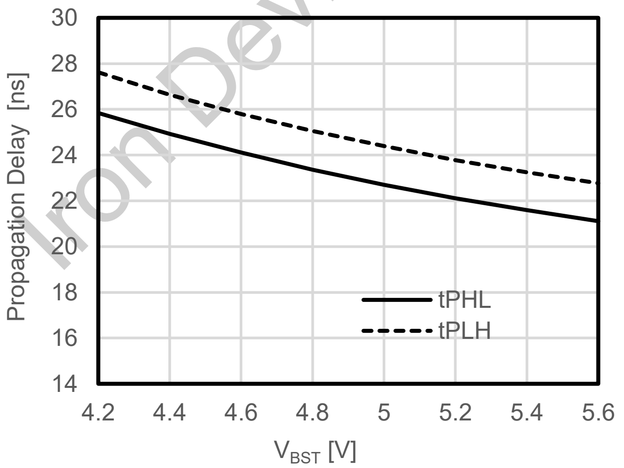


Figure 26. INH Propagation Delay vs. Supply Voltage (V_{DD}=V_{BST})

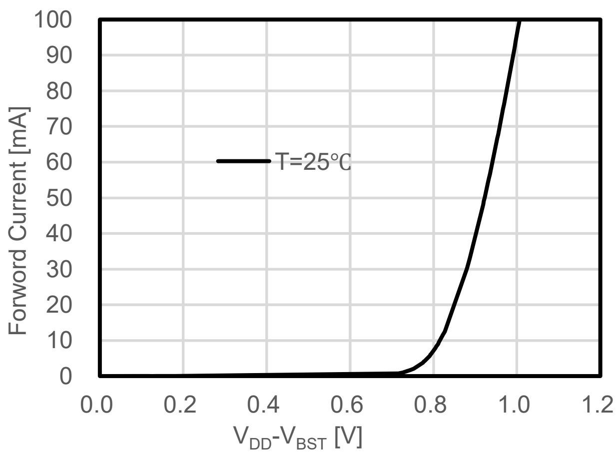


Figure 27. Bootstrap Diode Forward Voltage

Parameter Measurement Definitions

Switching Time Dsefinition

Propagation Delay Time

Figure 28 shows the switching time waveforms definitions of the turn−on (t_{PLH}) and turn−off (t_{PHL}) propagation delay times among the driver's two input signal INH, INL and two output signals HO (HOP, HON), and LO (LOP, LON). The typical values of the propagation delay (t_{PLH}, t_{PHL}), delay matching between channels times (MT).

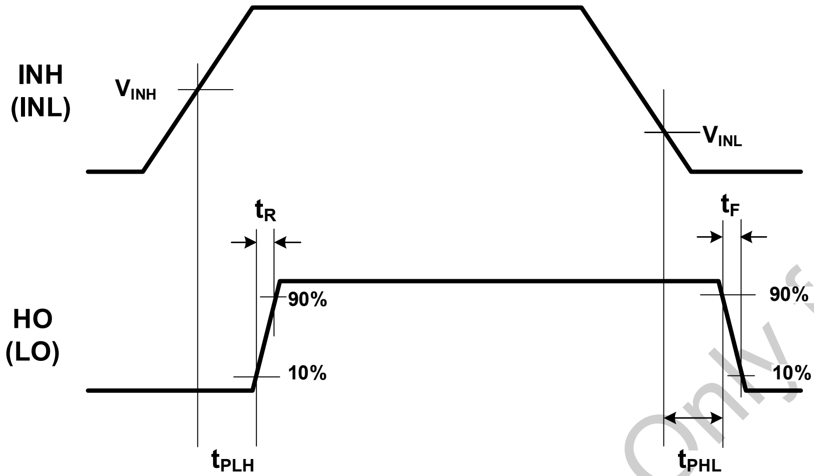


Figure 28. Switching Time Definition

Dead-Time Definition in PWM input mode

The SMA6533 provides dead-time control features to avoid shoot-through conditions that both high-side and low-side switches are turned-on simultaneously in PWM input mode. The dead-time is automatically inserted between two output signals (between HO and LO signals) according to setting dead times (t_{DTP} and t_{DTN}) as shown in Figure 29.

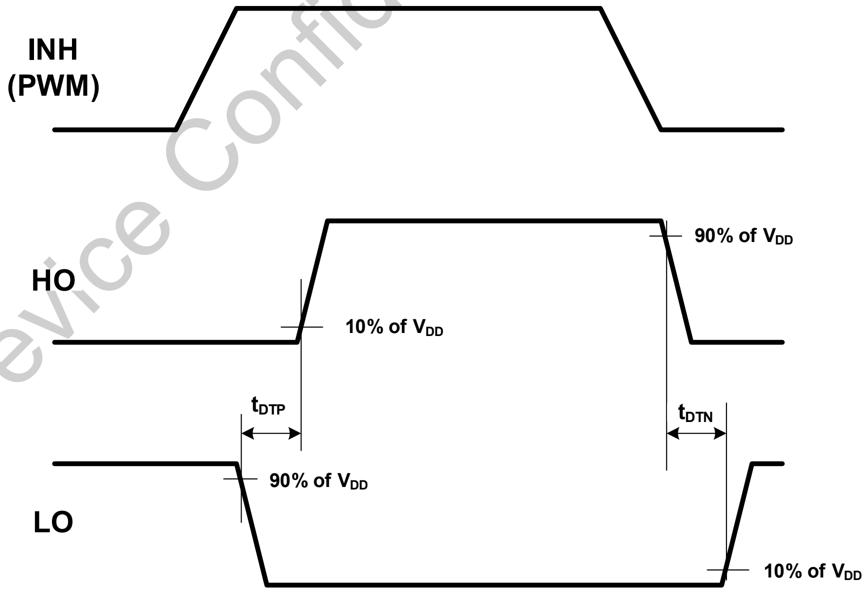


Figure 29. Dead-Time Definition in PWM input mode

Device Functional Description

Device Functional Mode Table

SMA6533 controls the output pins HOP, HON, LOP, and LON based on the input pins MODE, INH, and INL, as detailed in Table 1.

Table 1. Input and Output Logic Table

MODE	INH	INL	HOP	HON	LOP	LON
L	L	L	Open	L	Open	L
L	L	H	Open	L	H	Open
L	H	L	H	Open	Open	L
L	H	H	Open	L	Open	L
H	L	L	Open	L	Open	L
H	L	H	Open	L	H	Open
H	H	L	Open	L	Open	L
H	H	H	H	Open	Open	L

Notes
11) Open means Hi-z mode

Input Signal Configuration

SMA6533 enables configuration of the input signal through the MODE pin. The input signal configuration logic table and timing chart according to the MODE, INH and INL signals as shown in Table 2 and Figure 30.

Table 2. Input Signal Configuration Logic Table

MODE	INH	INL	DEAD-TIME	OUTPUT	Input Configuration
L	X	X	Disable	Enable	Dual-Input, Dual-Output in independent input mode
H	X	L	Disable	Disable	Single-Input, Dual-Output in single PWM input mode (Device is disable by INL)
H	X	H	Enable	Enable	Single-Input, Dual-Output in single PWM input mode (Device is enable by INL)

Notes
12) X means don't care

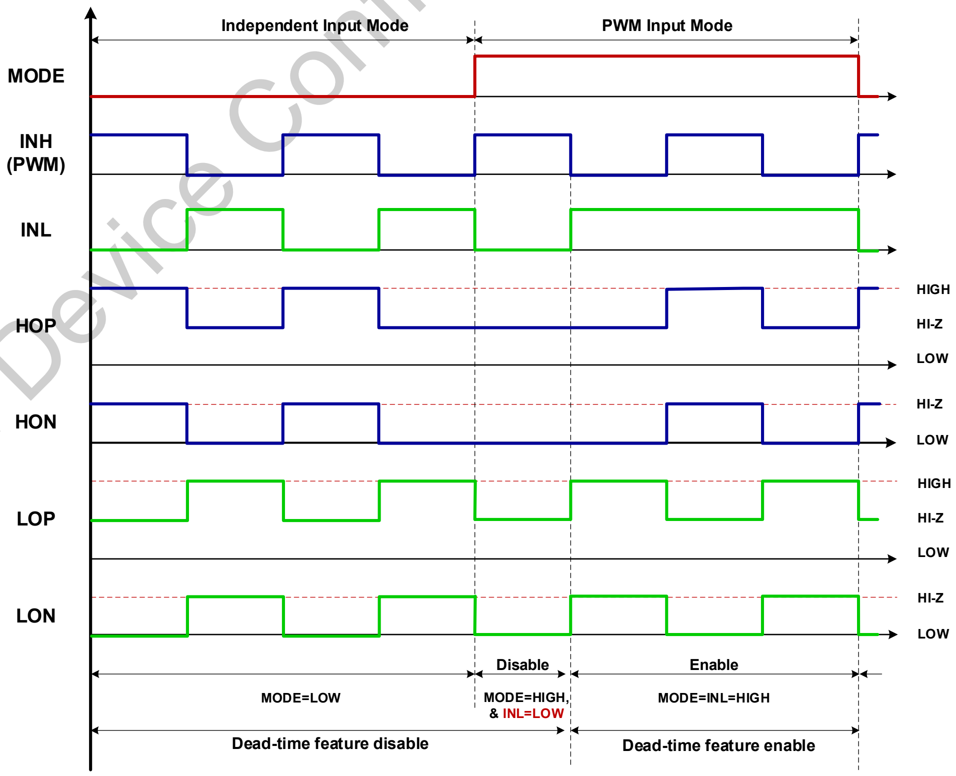


Figure 30. Timing Chart of Operation MODE Control

Input to Output Overall Operation

The SMA6533 provides important function such as independent undervoltage lockout (UVLO) protection for both high-side and low-side gate drivers and output status control. Figure 31 shows an overall input to output timing chart according to the MODE, INH and INL signals. Show the Under−Voltage Lockout (UVLO) protection events on the low-side and high-side power supplies, V_{DD} and V_{BST}, in the CASE−A, and B.

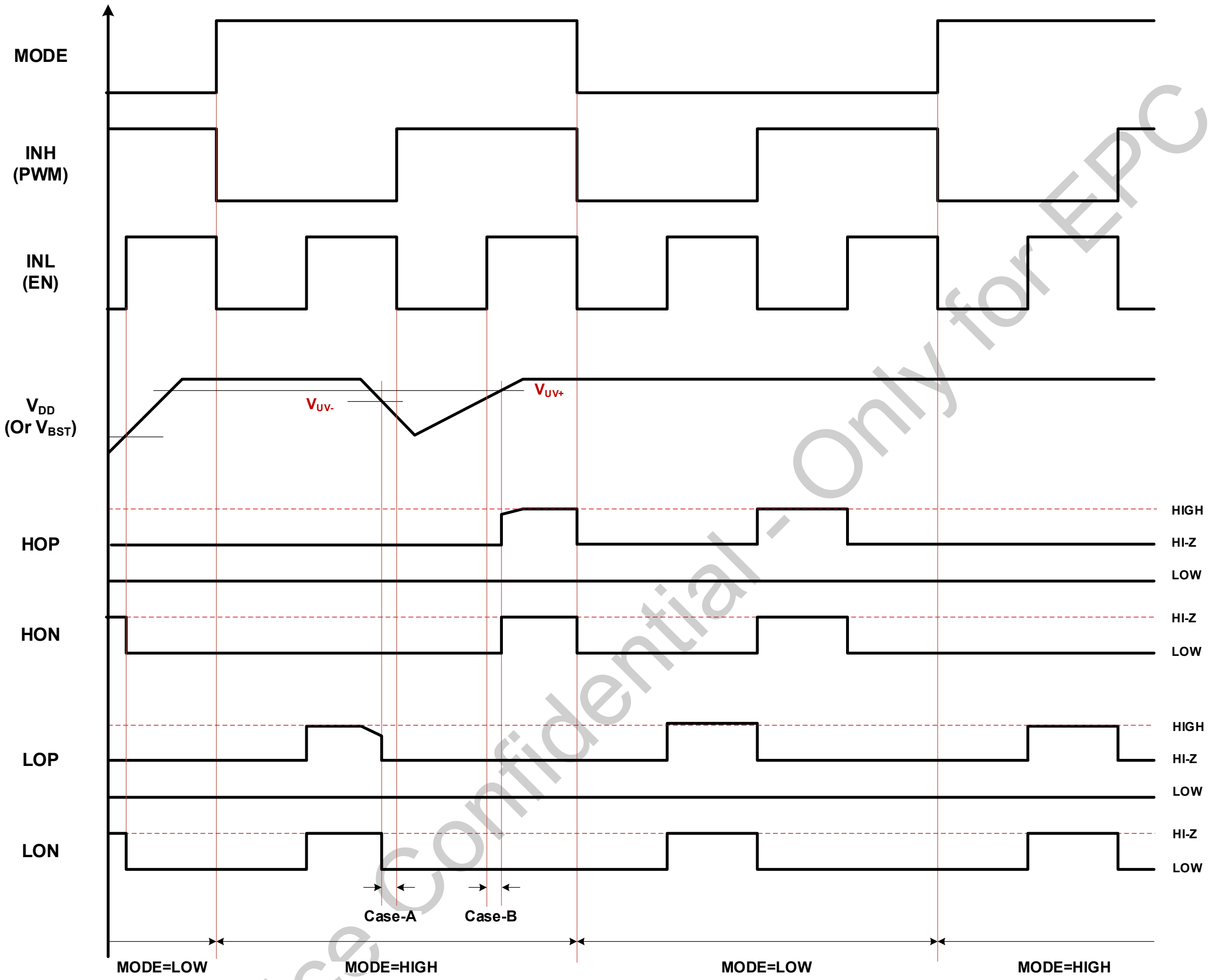
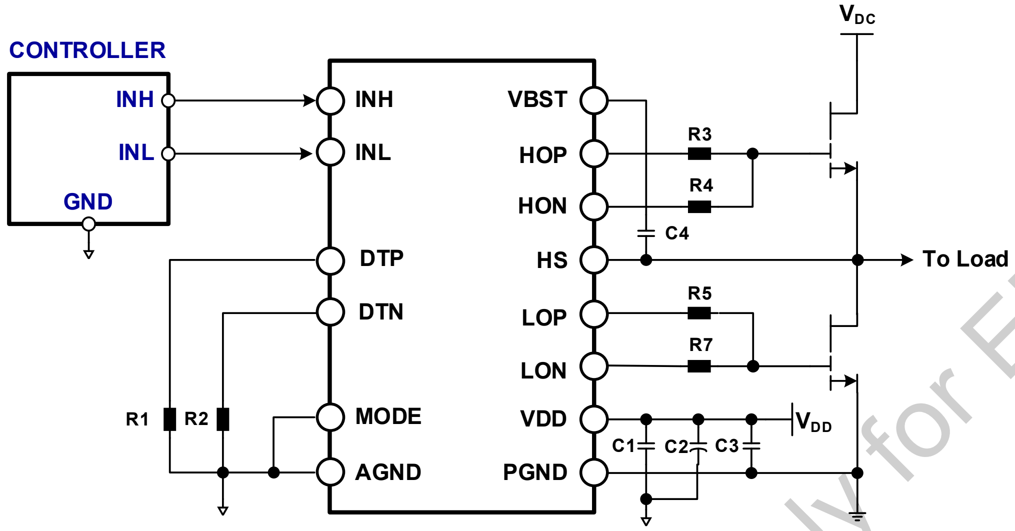


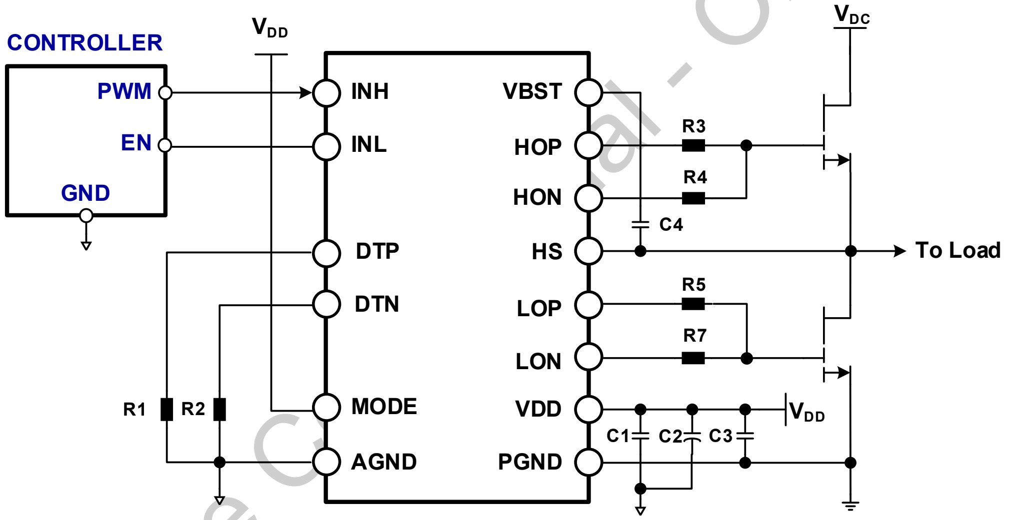
Figure 31. Timing Chart of an Overall Operation

Application Information

Typical Application Circuit



(a) In case of MODE = LOW in Independent Input Mode



(b) In case of MODE=INHIGH in Single PWM Input Mode

Figure 32. Typical Application Circuit

Table 3. Recommended Components

Components	Description	Specification
C1, C2	Low-side Driver Supply Capacitor.	The local power supply bypass capacitor recommended using 2 capacitors; a 100 nF ceramic surface−mount capacitor between V_{DD} and AGND pins which can be very close to the pins of the device, and another surface−mount capacitor of few microfarads added in parallel.
C3	Low-side Driver Bypass Capacitor.	The bypass capacitor, C3, between V_{DD} and PGND pins recommended a value of at least ten times the gate capacitance of power device, and no less than 100 nF and located as close to the device as possible.
C4	Bootstrap Capacitor	Place the capacitor as close as possible between the VBST and HS pins. The capacitor leakage current is important only if an electrolytic capacitor is used; otherwise, this can be neglected.
R1, R2	Dead-time Setting Resistors (DTP and DTN pins)	Dead-time setting resistance between high-side and low-side outputs in PWM input mode. $R_{DTP}\,[K\Omega] = (t_{DTP}[ns] + 0.2) \times 5.9$ $R_{DTN}\,[K\Omega] = (t_{DTN}[ns] + 1.72) \times 7$

Power Supply Recommendations

The recommended local bias supply voltage range for SMA6533 is from 4.5-V to 5.5-V between V_{DD} and AGND pins. The lower end of this range is governed by the internal UVLO protection feature of the V_{DD} supply circuit.

We recommend that the two separated bypass capacitors should be placed between the V_{DD} and AGND and PGND pins respectively, which is a low ESR, ceramic surface mount capacitor is necessary. The local power supply bypass capacitor recommended using 2 capacitors; a 100 nF ceramic surface−mount capacitor between V_{DD} and AGND pins which can be very close to the pins of the device, and another surface−mount capacitor of few microfarads added in parallel, C1 and C2 as shown in Figure 6. The other bypass capacitor, C3, between V_{DD} and PGND pins recommended a value of at least ten times the Gate capacitance of power device, and no less than 100 nF and located as close to the device as possible for the purpose of decoupling as shown in Figure 33.

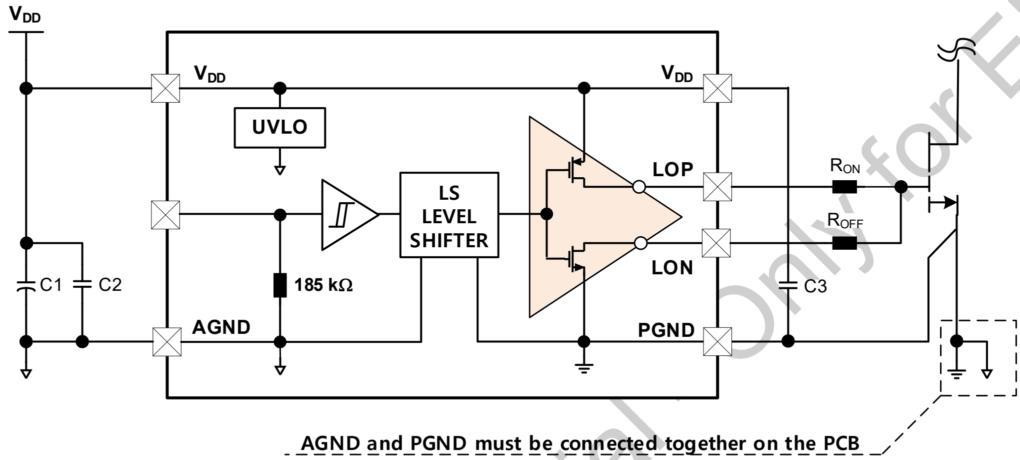


Figure 33. Application Schematic, Kelvin Gate Return Connections Example

Signal Ground (AGND) and Power Ground (PGND)

AGND is the ground for all internal control logic, under-voltage lockout (UVLO) circuitry and digital inputs. Internally, the AGND and PGND pins are separated from each other. PGND serves as the low−side, gate drive, return reference. For GaN FETs that include a source Kelvin return, a direct connection should be made from PGND to the GaN FET Kelvin return. For GaN FETs that do not include a dedicated source Kelvin pin, best practice PCB layout techniques should be used to isolate the gate drive return current from the power stage, ground return current. For half-bridge power topologies or applications with a current sense transformer, connect AGND and PGND on the PCB. In such applications, it is recommended to connect the AGND and PGND pins together with a short, low−impedance trace on the PCB as close to the SMA6533 as possible. For low−power applications, such as the active−clamp flyback or forward converter, a current sensing resistor, R_{CS}, located in the low−side GaN FET source leg is commonly used. For these applications, the SMA6533 PGND and AGND pins should remain unconnected on the PCB, as connecting them would result in R_{CS} being shorted, as shown in Figure 32.

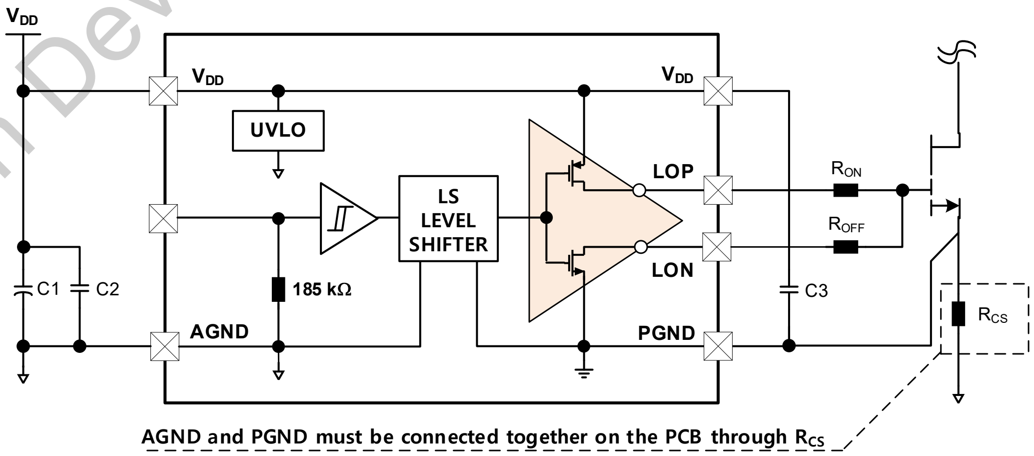


Figure 34. Application Schematic, Shunt Resistor Current Sense Example

Input Stage Structure

The input signal pins (INH, INL, and MODE) of the SMA6533 are based on the TTL compatible input−threshold logic that is independent of the V_{DD} supply voltage. The logic level compatible input provides a typically high and low threshold of 1.9 V and 1.4 V respectively. The input signal pins impedance of the SMA6533 is 185 kΩ typically and the INH, INL, and MODE pins are pulled to AGND pin as shown in Figure 35. It is recommended that MODE pin should be tied to V_{DD} or AGND pins to achieve better noise immunity, if the MODE pin is not used because the MODE pin is quite responsive, as far as propagation delay and other switching parameters are concerned. An RC filter is recommended to be added on the input signal pins, INH, INL, and MODE, to reduce the impact of system noise and ground bounce, the time constant of the RC filter. Such a filter should use an R_{IN}, R1, R2, and R3, in the range of 0 Ω to 100 Ω and a C_{IN}, C4, C5, and C6, in the range of 10 pF and 100 pF as shown in Figure 35.

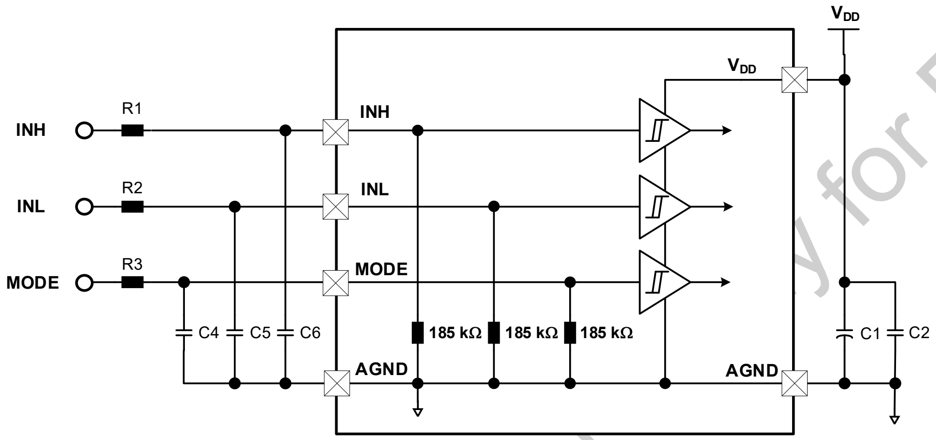


Figure 35. Input Stage Structure

Dead-Time Control Function in PWM Input Mode

The SMA6533 provides dead-time control features to avoid shoot-through conditions that both high-side and low-side switches are turned-on simultaneously in single PWM input mode. The dead-time is set individually by dead-time setting resistance (R_{DTP} and R_{DTN}). The characteristic curve and timing charts are shown in Figure 24, Figure 25 and Figure 36. The dead-time between the two outputs can be calculated as follows.

$$R_{DTP}\,[K\Omega] = (t_{DTP}[ns] + 0.2\,) \times 5.9$$

$$R_{DTN}\,[K\Omega] = (t_{DTN}[ns] + 1.72) \times 7$$

where,

R_{DTP} = Dead-time control resistor for t_{DTP}

R_{DTN} = Dead-time control resistor for t_{DTN}

t_{DTP} = Dead-time (LO falling to HO rising)

t_{DTN} = Dead-time (HO falling to LO rising)

Note that the VBST-HS voltage is calculated based on a forward voltage drop 0.7 V for the built-in bootstrap diode.

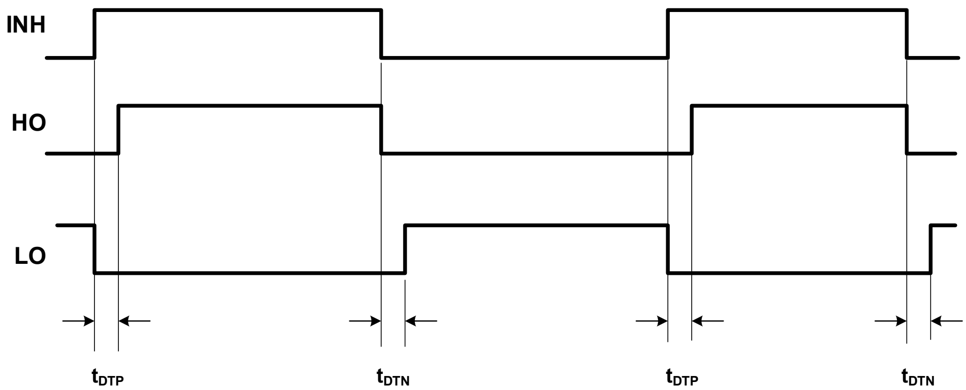


Figure 36. Timing Chart of the Dead-Time Control Function in PWM input mode

Output Stage Structure

The output driver stage of the SMA6533 features a pull-up and pull-down structure. The pull up structure of the consist of a PMOS stage ensuring to pull all the way to the VDD rail and the pull-down structure of the consists of a NMOS device as shown in Figure 37. The output voltage swing between VDD and PGND provides rail-to-rail operation. The SMA6533 output stages is designed to support split turn-on (LOP and HOP) and turn-off (LON and HON) output pins respectively as shown in Figure 10. This scheme allows a flexibility to adjust the turn-on and turn-off speed as well as fine tuning dV_{DS}/dt turn−on and turn−off transitions by independently adding additional impedance in either the turn-on or the turn-off path.

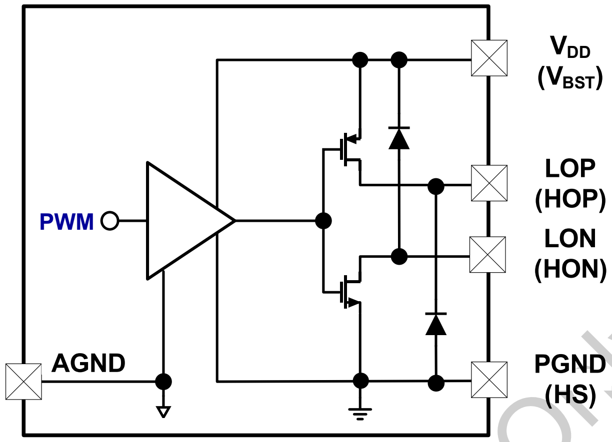


Figure 37. Output Stage Structure

Bootstrap Supply Considerations

Consideration of Bootstrap Circuit Design

The gate driver and the ground referenced control signal are linked by a level shift circuit that must tolerate the high−voltage difference and considerable capacitive switching currents between the floating high−side and ground−referenced low−side circuits. The high−voltage gate−drive ICs are differentiated by unique level−shift design. To maintain high efficiency and manageable power dissipation, the level−shifters should not draw any current during the on−time of the main switch. The bootstrap circuit is useful in a high−voltage gate driver and operates as follows. When the HS pin goes below the local supply voltage V_{DD} or is pulled down to ground (the low−side switch is turned on and the high−side switch is turned off), the bootstrap capacitor, C_{BOOT}, charges through the bootstrap diode, D_{BOOT}, from the V_{DD} power supply, as shown in Figure 38. This is provided by V_{BST} when HS pin is pulled to a higher voltage by the high−side switch, the V_{BST} supply floats and the bootstrap diode reverses bias and blocks the rail voltage (the low−side switch is turned off and high−side switch is turned on) from the local supply voltage, V_{DD}. The bootstrap circuit can be considered in the half-bridge structure to supply V_{DD} as an inexpensive and simple solution. But it has some limitations, such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor, C_{BOOT}. The current path of charging and discharging C_{BOOT} is describes in Figure 38. when the high-side driver supply V_{BST} goes below the low-side driver supply V_{DD} in the Bootstrap Circuit. (Q2 is turned on and Q1 is turned off). The C_{BOOT} charges through the bootstrap diode (D_{BOOT}) from the V_{DD} power supply, as shown in Figure 38. When Q2 is turned off and Q1 is turned on, charged voltage on C_{BOOT} floats and D_{BOOT} protects low-side driver supply (V_{DD}) from DC rail voltage after reverse recovery time. In addition, C_{BOOT} can be recharged during the low-side freewheeling recirculation even in the dead-time period when both Q1 and Q2 are turned off.

The biggest difficulty with this circuit is that the negative voltage present at the source of the switching device during turn−off causes load current to suddenly flow in the low−side freewheeling diode, as shown in Figure 38. This negative voltage can be trouble for the gate driver's output stage because it directly affects the source HS pin of the driver or PWM control IC and might pull some of the internal circuitry significantly below ground. The other problem caused by the negative voltage transient is the possibility to develop an over−voltage condition across the bootstrap capacitor. The bootstrap capacitor, C_{BOOT}, is peak charged by the bootstrap diode, D_{BOOT}, from V_{DD} the power source. Since the V_{DD} power source is referenced to ground (AGND), the maximum voltage that can build on the bootstrap capacitor is the sum of V_{DD} and the amplitude of the negative voltage at the source terminal.

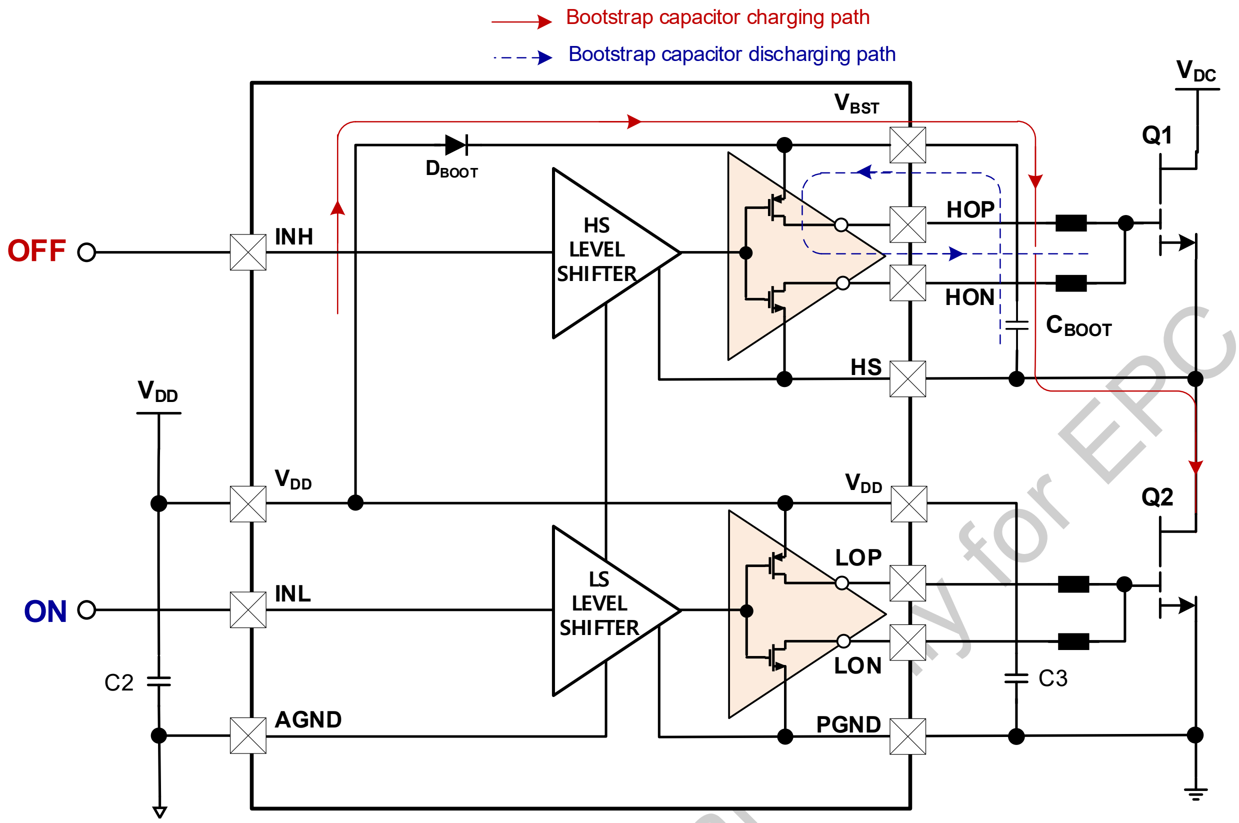


Figure 38. Current path of C_{BOOT} in the Bootstrap Circuit

Bootstrap Components

The duty−cycle is limited by the requirement to refresh the charge in the C_{BOOT}, and there are startup problems. The C_{BOOT} uses a low−ESR capacitor, such as ceramic capacitor. The capacitor from V_{DD} to AGND, (C2) supports both the low−side driver and bootstrap recharge. A local supply bypass capacitor (C2) value is recommended.at least ten times higher than the bootstrap capacitor (C_{BOOT}). The bootstrap diode (D_{BOOT}) should be designed to have a lower forward voltage drop and switching time as soon as possible to fast recovery time.

Select the Bootstrap Capacitor

The C_{BOOT} is charged with repetitive cycle while V_{BST} of high-side driver goes below the V_{DD} supply of low-side driver after turning on the low−side driver. The bootstrap capacitor is discharged only when the high−side switch is turned on. If the voltage charged in C_{BOOT} is defined as V_{BST}. Consider the maximum allowable VBST voltage drop required to drive the MOSFET properly. The maximum allowable voltage drop (V_{BST}) depends on the minimum gate drive voltage (for the high−side switch). The value of bootstrap capacitor can be obtained with the below equation.

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BST}}$$

Where, Q_{TOTAL} is the total amount of the charge supplied by the capacitor.

The total charge supplied by the bootstrap capacitor is as shown in the below equation.

$$Q_{TOTAL} = Q_{GATE} + \left(I_{LKCAP} + I_{LKGS} + I_{LK} + I_{QVBST} + I_{LKDIODE}\right) \times t_{ON}$$

where:

Q_{GATE} = Total gate charge.

I_{LKGS} = Switch gate−source leakage current.

I_{LKCAP} = Bootstrap capacitor leakage current.

I_{LK} = Bootstrap circuit leakage current.

I_{QVBST} = Quiescent current of gate driver.

t_{ON} = High−side switch on time; and

$I_{LKDIODE}$ = Bootstrap diode leakage current.

The capacitor leakage current is important only if an electrolytic capacitor is used; otherwise, this can be neglected.

HS Negative Voltage and Bootstrap Supply Voltage Clamping

Bootstrap Clamping due to the intrinsic feature of the enhancement mode GaN FETs, the source-to-drain voltage of the low-side MOSFET is usually higher than the diode forward voltage drops when the gate is pulls low. This causes a negative voltage to appear on the HS pin. Moreover, this negative voltage transient on HS can be significantly high, depending on the board layout and the parasitic inductances of the device's drain and source, L_{S1} and L_{S2} as shown in . When the high-side driver uses the floating bootstrap configuration, a negative HS voltage can lead to an excessive bootstrap voltage, which can damage the high-side GaN FET. The SMA6533 solves this problem with an internal clamping circuit that prevents the bootstrap supply voltage from exceeding 5.75 V typically.

Power Dissipation Considerations

Estimating Gate Driver Power Loss

The supply current at a given channel of gate driver is a function of the supply voltage, switching frequency, and output load. In general, gate driving total power loss, P_{GDRV}, consist of static power loss, P_{GD}, and dynamic power loss, P_{GDSW}. Bootstrap diode loss is not included in total loss, P_{GDRV}, and not discussed in this section. The first component is static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as self-power consumption when operating switching frequency. P_{GD} is measured on the bench with no load connected to low-side and high-side outputs at a given V_{DD}, and V_{BST}, switching frequency and ambient temperature.

$$P_{GD} = (V_{DD} \times I_{DDO}) + (V_{BST} \times I_{VBSTO})$$

where: I_{DDO} and I_{VBSTO} are measured current at high and low-side gate driver supply voltages (V_{DD} and V_{BST}) and target switching frequency. The second component is the dynamic operation loss, P_{GDSW}, with load capacitance which the driver charges and discharges the load during each switching cycle.

For example, the value of dynamic operation loss, P_{GDSW}, can be obtained by gate charge.

$$P_{GDSW} = (V_{DD} \times Q_G \times f_{SW}) + (V_{BST} \times Q_G \times f_{SW})$$

where: Q_G is the total gate charge of switching device. f_{SW} is the switching frequency.

Therefore, total gate driving power loss, P_{GDRV}, can be calculated

$$P_{GDRV} = P_{GDQ} + P_{GDSW} \text{ [W]}$$

In this example, V_{DD} = 5 V, V_{BST} = 5 V and Q_G = 5 nC. The current on each power supply, with INH and INL switching from 0 V to 5 V at 500 kHz, is measured to be I_{DDO} = 0.5 mA, and I_{VBSTO} = 0.5 mA.

$$P_{GDRV} = P_{GD} + P_{GDSW} = (5V \times 0.5mA) + (5V \times 0.5mA) + (2 \times 5V \times 5nC \times 500kHz) = 30\text{ mW}$$

The gate driver loss on the output stage, P_{GDO}, is part of P_{GDSW}. P_{GDO} will be equal to P_{GDSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the gate driver.

If there are external turn-on and turn-off resistances, this power dissipation is shared between the internal on resistances of the gate driver switches and the external gate resistances, R_{ON} and R_{OFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the gate drive chips per channel

$$P_{GDO} = \frac{P_{GDSW}}{2} \times \left(\frac{R_{PMOS}}{R_{ON} + R_{GFET\_int}} + \frac{R_{NMOS}}{R_{OFF} + R_{GFET\_int}}\right)$$

Therefore, total gate driver loss dissipated in the gate driver, P_{GDRV}, is:

$$P_{GDRV} = P_{GD} + P_{GDO} \text{ [W]}$$

Estimating Junction Temperature

Taking the power dissipation found inside the chip and multiplying it by $R_{\theta JA}$ gives the rise above ambient temperature that the gate driver can be estimated with:

$$T_J = R_{\theta JA} \times P_{GDRV} + T_A \text{ Or}$$
$$T_J = T_C + \psi_{JT} + P_{GDRV}$$

where: $R_{\theta JA}$ is the thermal resistance junction−air from the thermal information table in datasheet.
T_C is the gate drive IC case-top temperature measured with a thermocouple or some other instrument.

Ψ_{JT} is the Junction-to-top characterization parameter from the thermal information table in datasheet. For the device to remain within specification, T_J must not exceed 125°C.

Layout

Layout Guidelines for Enhanced Mode GaN FETs

Enhancement-mode GaN FETs feature low gate charge and minimal Miller capacitance, enabling high-speed switching performance. However, the resulting high dv/dt and di/dt, combined with a low gate threshold voltage and limited gate voltage margin, necessitate careful PCB layout to ensure optimal device operation and reliability. To minimize gate loop inductance and prevent false triggering, the gate driver should be placed close to the FET with short, low-inductance traces. Proper decoupling and power loop optimization are essential to suppress voltage overshoot and EMI.
To optimize performance, the following layout recommendations:

1. ***Minimize Gate Drive Loop Area***
   The first consideration in driver layout design is to minimize the physical area of the high-current gate charge/discharge loop. This reduces loop inductance and mitigates noise coupling at the GaN FET gate terminal. To achieve optimal performance, the GaN FETs should be placed close to the driver.
2. ***Optimize Bootstrap Loop***
   The second high-current loop consists of the bootstrap capacitor, the ground-referenced VDD bypass capacitor, and the low-side GaN FET. During each switching cycle, the bootstrap capacitor is recharged through the bootstrap diode from the VDD bypass capacitor. This recharge event occurs over a short duration and involves high peak current. To ensure reliable operation and minimize parasitic effects, the physical length and area of this loop must be kept as small as possible.
3. ***Minimize Source Inductance Impact***
   The parasitic inductance in series with the source terminals of the high-side and low-side FETs can induce excessive negative voltage transients at the driver. To mitigate this, Iron Device recommends connecting the HS and VSS pins directly to the respective source terminals using short, low-inductance traces. This minimizes voltage stress on the driver and ensures robust switching performance.
4. ***Suppress Gate Ringing***
   The combination of parasitic source inductance, gate capacitance, and the driver's pull-down path can form an LCR resonant circuit, leading to gate voltage oscillations. To suppress this ringing and ensure stable gate operation, an optional series gate resistor between the driver and the FET gate.
5. ***Strategic Placement of Decoupling and Bootstrap Capacitors***
   Low-ESR and low-ESL capacitors must be placed close to the IC, between the VDD and PGND pins, and between the HB and HS pins, to support the high peak current drawn from VDD during FET turn-on. While minimizing the gate driver loop remains the highest priority, it is also recommended to place the VDD decoupling capacitor and the HB–HS bootstrap capacitor on the same side of the PCB as the driver. Avoiding vias in these high-current paths is critical, as via inductance can introduce excessive ringing at the IC pins.
6. ***Input Power Bus Decoupling***
   To suppress ringing on the input power bus, low-ESR ceramic capacitors should be placed as close as possible to the GaN FETs. These capacitors help to support high-frequency transient currents and maintain power rail stability during switching events.

Layout Example

Figure 39 shows recommended layout for SMA6533 with turn-on and off gate resistors.

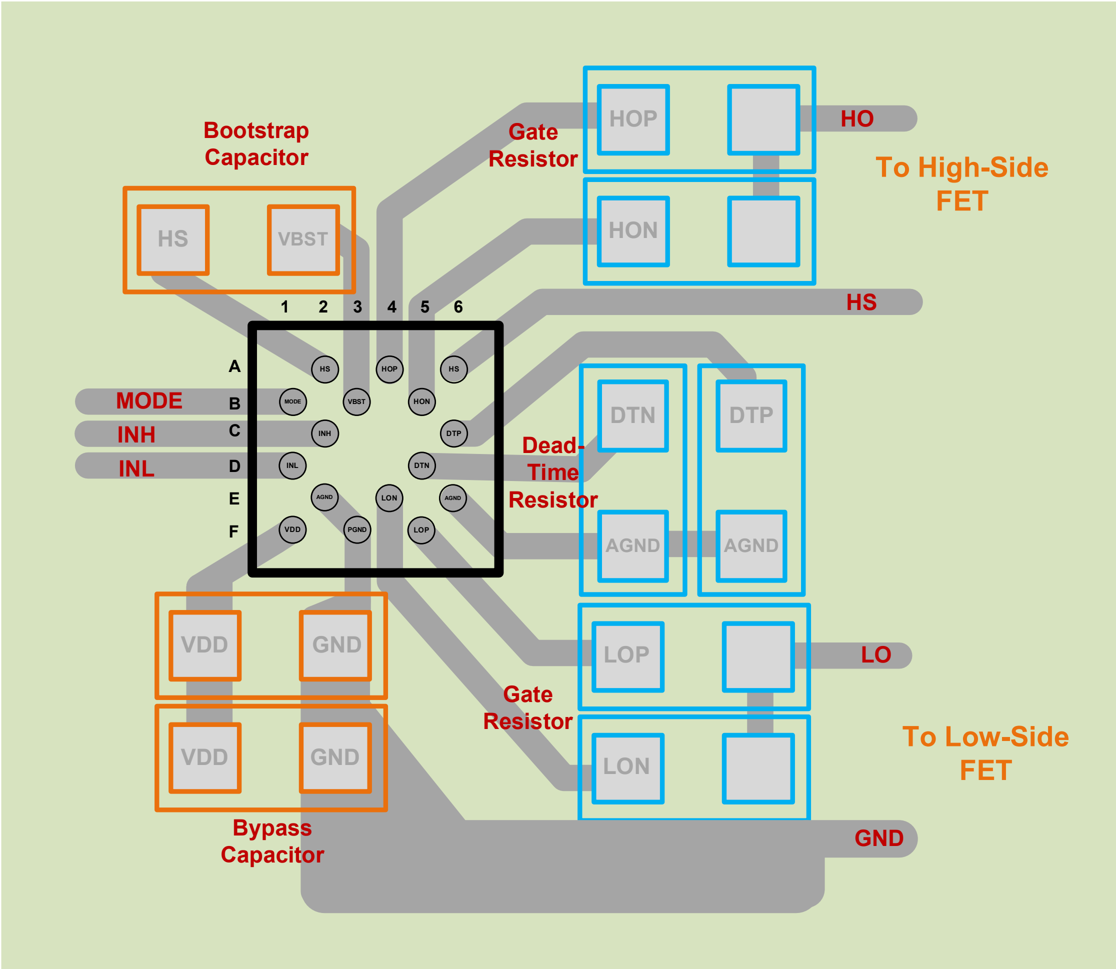


Figure 39. Layout Example with HO and LO Gate Resistors

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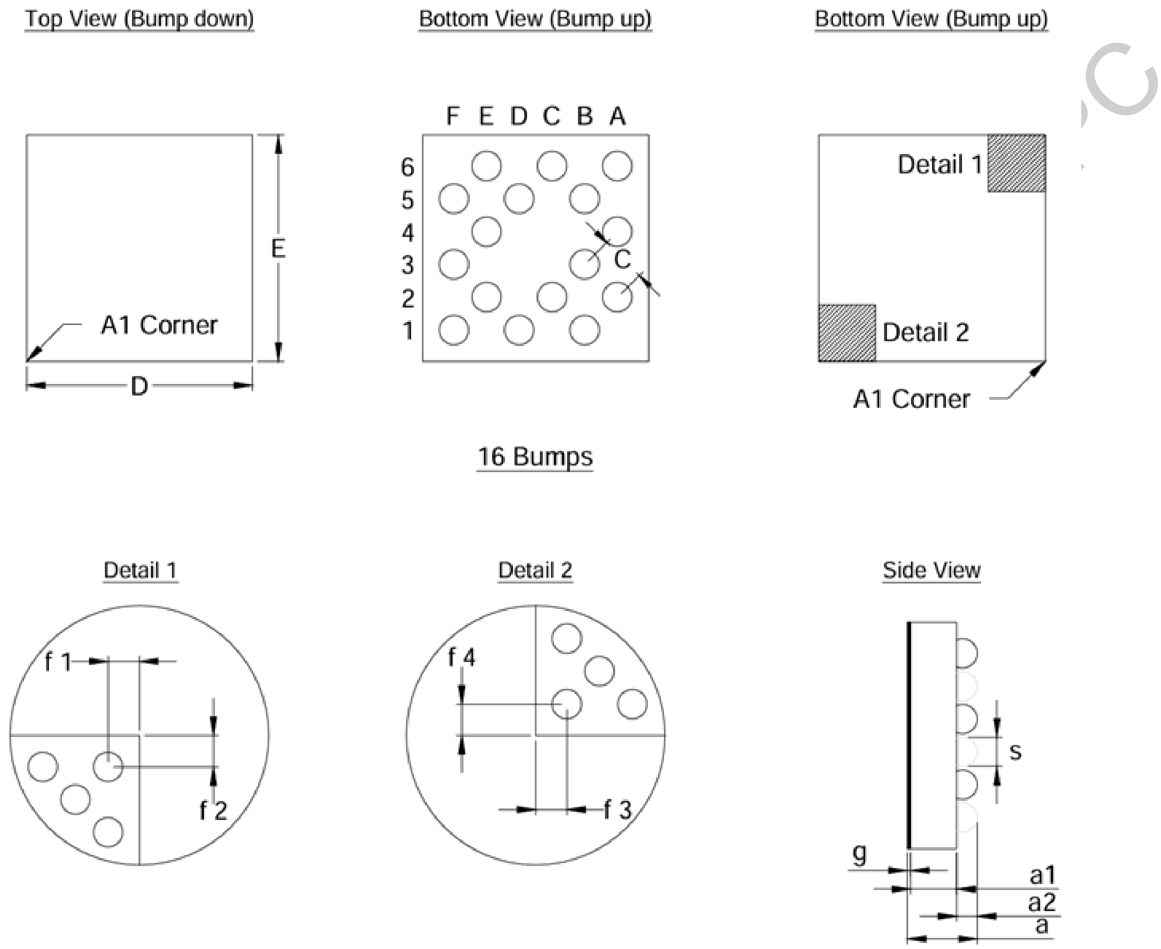
Notes
13) E2 and E6 (AGND) , A2 and A6 (HS) pins are internally connected

Package Information

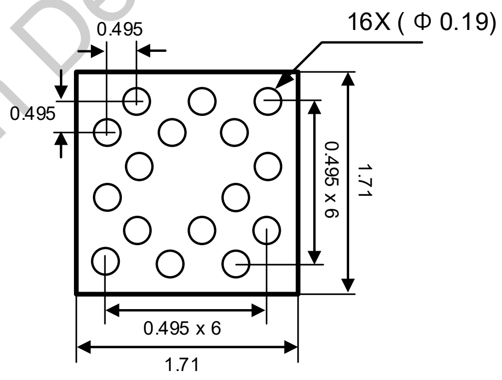
Orderable Device	Package Type	Pins	Temp. Range	Eco Plan
SMA6533-W	WLCSP	16	-40 °C to +125 °C	Pb-Free / RoHS

Dimensions are in millimeters, unless otherwise specified.

WLCSP



RECOMMENDED MOUNTING FOOTPRINT



Package Size (D x E)		D = 1710 ± 30	E = 1710 ± 30
Package Thickness (a)		530 ± 30	
Wafer Thickness (a1)		350 ± 12	
Ball Height (a2)		155 ± 15	
Back Side Coating Thickness (g)		25 ± 3	
Ball Pitch (C)		350	
Ball Diameter (s)		220 ± 25	
Distance From Bump Center To Package Edge	f1	236.25	
	f2	236.25	
	f3	236.25	
	f4	236.25	
Customer POD Drawing No. / Rev. No.		N/A	

- Bump is Facing Up(Bottom View)

Revision History

Revision Number	Date	Notes
1.00	2025.10.14.	Initial release.